CLAIMS:

1. A circuit for synchronizing two signals triggered by clocks of different frequencies, comprising:

a recording circuit for recording sampling states of a higher frequency clock at a positive edge and a negative edge; and

a sampling circuit for sampling a lower frequency write-enable signal at opposite edges of the positive edge and the negative edge according to the states, and joining sampling results respectively sampled from the positive edge and the negative edge to output a synchronized output signal.

2. The circuit of claim 1, wherein the recording circuit comprises:

a first D-type flip-flop, which is positive-edge triggered, for recording the state at the positive edge of the higher frequency clock, wherein the first D-type flip-flop has a D terminal for receiving the lower frequency write-enable signal, a CK terminal for receiving the higher frequency clock, and a Q terminal connected externally and with an initial state 0; and

a second D-type flip-flop, which is positive-edge triggered, for recording the state at the negative edge of the higher frequency clock, wherein the second D-type flip-flop has a D terminal for receiving the lower frequency write-enable signal, a CK terminal for receiving an inverse state of the higher frequency clock, and a Q terminal connected externally and with an initial state 0.

3. The circuit of claim 2, wherein the Q terminal of the first D-type flip-flop has an output 0 means that a state at the positive edge of the higher frequency clock is a sampling state, whereas an output is 1 means that the state is a lock state.

4. The circuit of claim 2, wherein an output of the Q terminal of the second D-type flip-flop is 0 means that a state at the negative edge of the higher frequency clock is a sampling state, whereas an output is 1 means that the state is a lock state.

5. The circuit of claim 1, wherein the sampling circuit comprises:

a first AND-gate having an input terminal for receiving the lower frequency write-enable signal, another input terminal for receiving an inverse state output by the Q terminal of the

first D-type flip-flop, and an output terminal connected externally;

a third D-type flip-flop, which is positive-edge triggered, for sampling from the lower frequency write-enable signal at the negative edge of the higher frequency clock, wherein the third D-type flip-flop has a D terminal for receiving signals output from the first AND-gate, a CK terminal for receiving an inverse state of the higher frequency clock, a Q terminal connected externally and with an initial state 0;

a second AND-gate having an input terminal for receiving the lower frequency write-enable signal, another input terminal for receiving an inverse state output by the Q terminal of the second D-type flip-flop, and an output terminal connected externally;

a fourth D-type flip-flop, which is positive-edge triggered, for sampling from the lower frequency write-enable signal at the positive edge of the higher frequency clock, wherein the fourth D-type flip-flop has a D terminal for receiving signals output by the second AND-gate, a CK terminal for receiving the higher frequency clock, and a Q terminal connected externally and with an initial state 0; and

an OR-gate having an input terminal for receiving an output of the Q terminal of the third D-type flip-flop, another input terminal for receiving an output of the Q terminal of the fourth D-type flip-flop, and an output terminal connected externally.

6. The circuit of claim 5, wherein the sampling circuit further comprises a fifth D-type flip-flop, which is positive-edge triggered, and has a D terminal for receiving signals output by the OR-gate, a CK terminal for receiving the higher frequency clock, and a Q terminal connected externally and with an initial state 0.

7. A method for synchronizing two signals triggered by clocks of different frequencies, comprising the steps of:

(a) initializing states at a positive edge and a negative edge of a higher frequency clock to be sampling states;

(b) sampling from a lower frequency write-enable signal at the positive edge and the negative edge of the higher frequency clock, respectively, and recording states at the positive edge and the negative edge of the higher frequency clock;

(c) sampling at a next opposite edge according to each state at the positive edge and the negative edge of the higher frequency clock,; and

(d) joining sampling results of the lower frequency write-enable signal obtained respectively at the positive edge and the negative edge of the higher frequency clock, and

outputting a synchronized write-enable signal.

8. The method of claim 7, wherein the states in the step (b) is changed according to that:

9. If the sampling result from the lower frequency write-enable signal at the positive edge or the negative edge of the higher frequency clock is 1, the state at the positive edge or the negative edge is changed to be a lock state, or if the sampling result is 0, the state at the positive edge or the negative edge is changed to be a sampling state.

10. The method of claim 8, wherein the sampling in the step (c) is performed according to that:

if a preceding positive edge of a current negative edge of the higher frequency clock is in a sampling state, the sampling result of the negative edge is valid, if the sampling result is 0, the output is 0, if the sampling result is 1, the output is 1, if the preceding positive edge is in a lock state, all sampling results at the negative edge are 0; and

if a preceding negative edge of a current positive edge of the higher frequency clock is in a sampling state, the sampling result of the positive edge is valid, if the sampling result is 0, the output is 0, if the sampling result is 1, the output is 1, if the preceding negative edge is in a lock state, all sampling results of the positive edge are 0.